TANCELL

5G FAT / SAT Test Report

Commissioning & Acceptance Engineering Package

Document owner	Tancell Engineering
Revision	1.0
Date	14 September 2026
Classification	Technical / Engineering Reference
Standards basis	3GPP 5GS / 5G NR; O-RAN architecture concepts

Important: This package is a Tancell engineering reference design. Test values marked 'sample' or 'simulated' are not third-party certification results and must be replaced by measured laboratory/site data before regulatory submission or customer acceptance.

Document scope

This document set defines a vendor-neutral 5G mobile integration baseline covering UE-to-RAN connectivity, radio unit integration, transport/fronthaul, synchronization, DC power, grounding, mechanical installation, commissioning, alarms and acceptance testing. It is intended for engineering, tender, installation and FAT/SAT preparation.

Reference standards

Primary architecture reference: 3GPP TS 23.501 (5G System architecture). Radio/base-station reference: 3GPP TS 38.104 / ETSI TS 138 104. Open RAN transport drawings use O-RAN split 7-2x concepts. Always validate band, power, emissions, EMC, electrical safety and local spectrum/licensing requirements for the target country.

1. FAT - factory acceptance

Sample test plots and check sequences for pre-deployment verification.

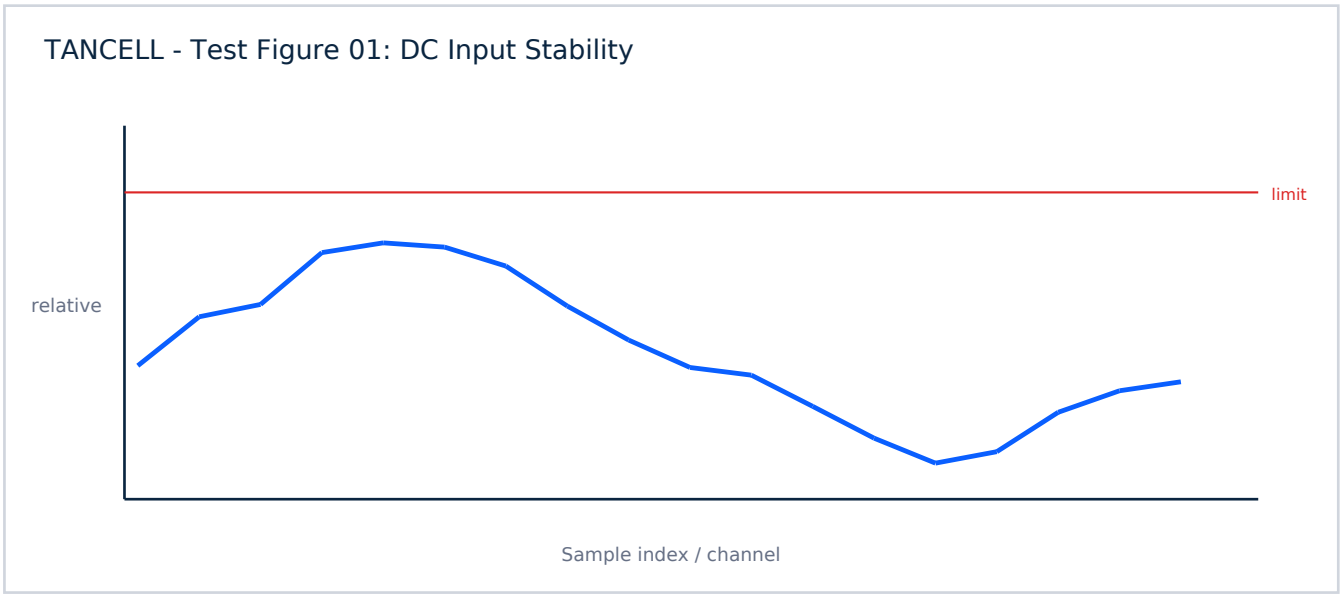

Figure 1. DC Input Stability. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

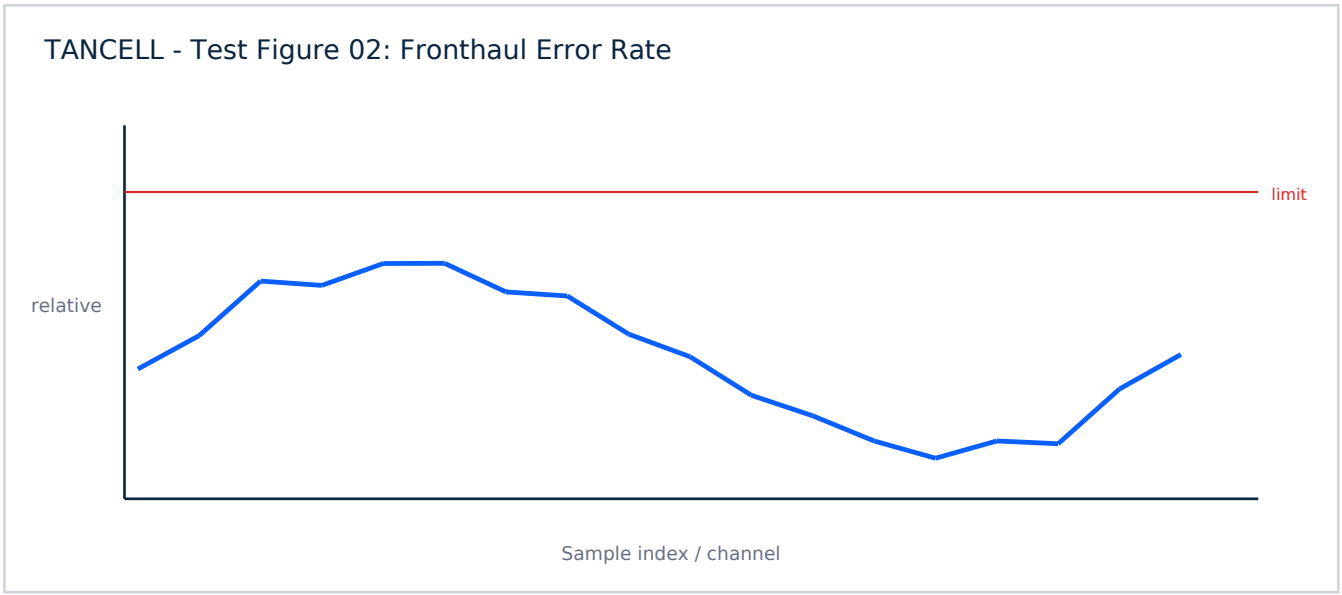

Figure 2. Fronthaul Error Rate. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

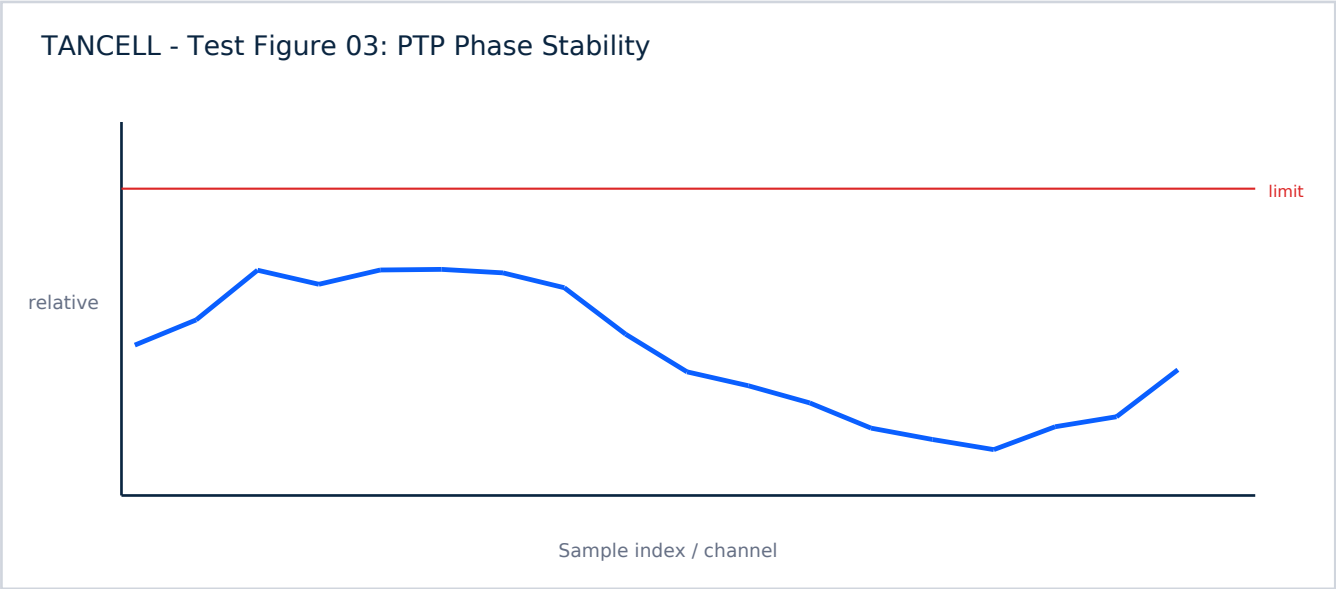

Figure 3. PTP Phase Stability. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

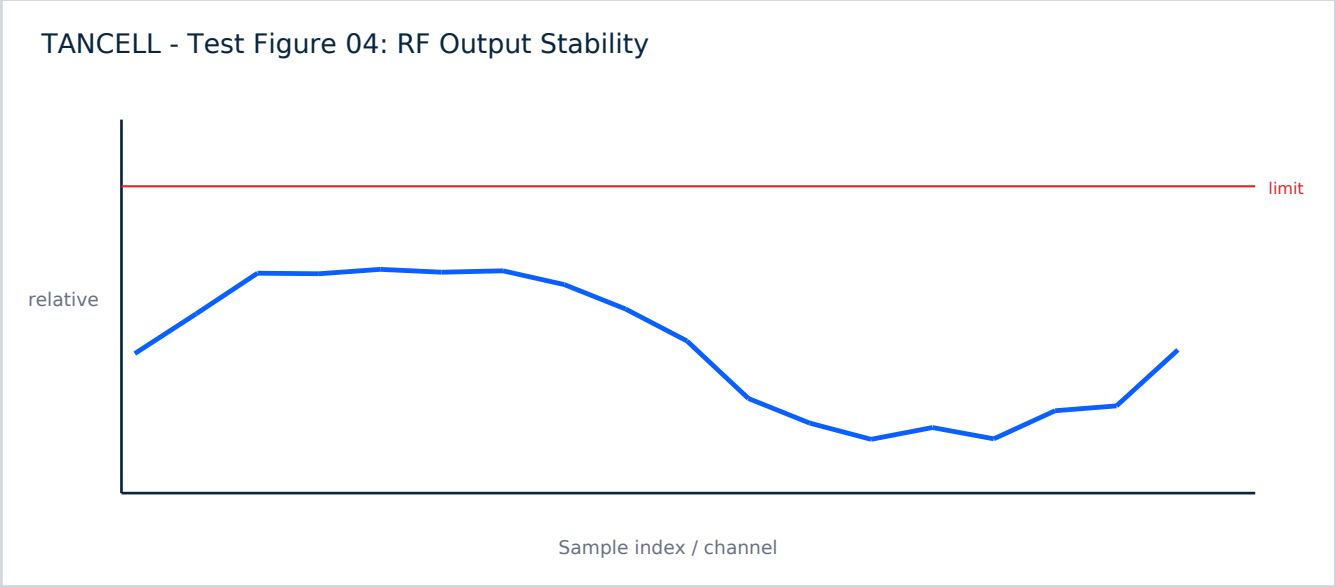

Figure 4. RF Output Stability. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

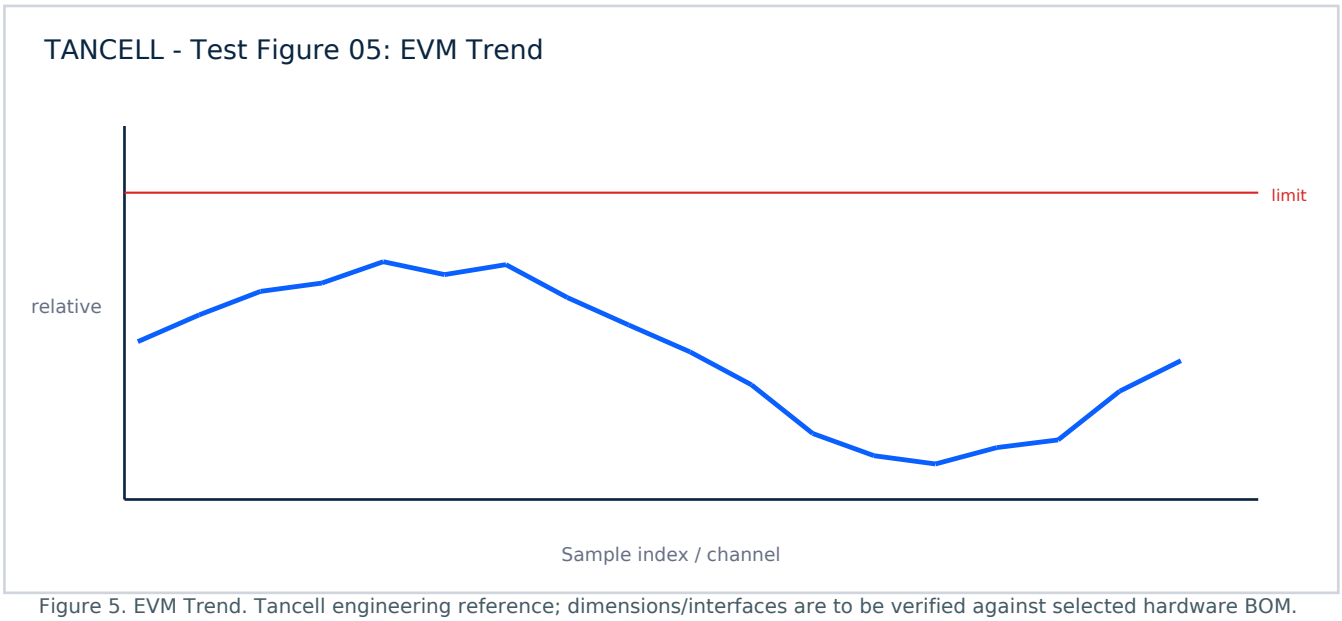

Figure 5. EVM Trend. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

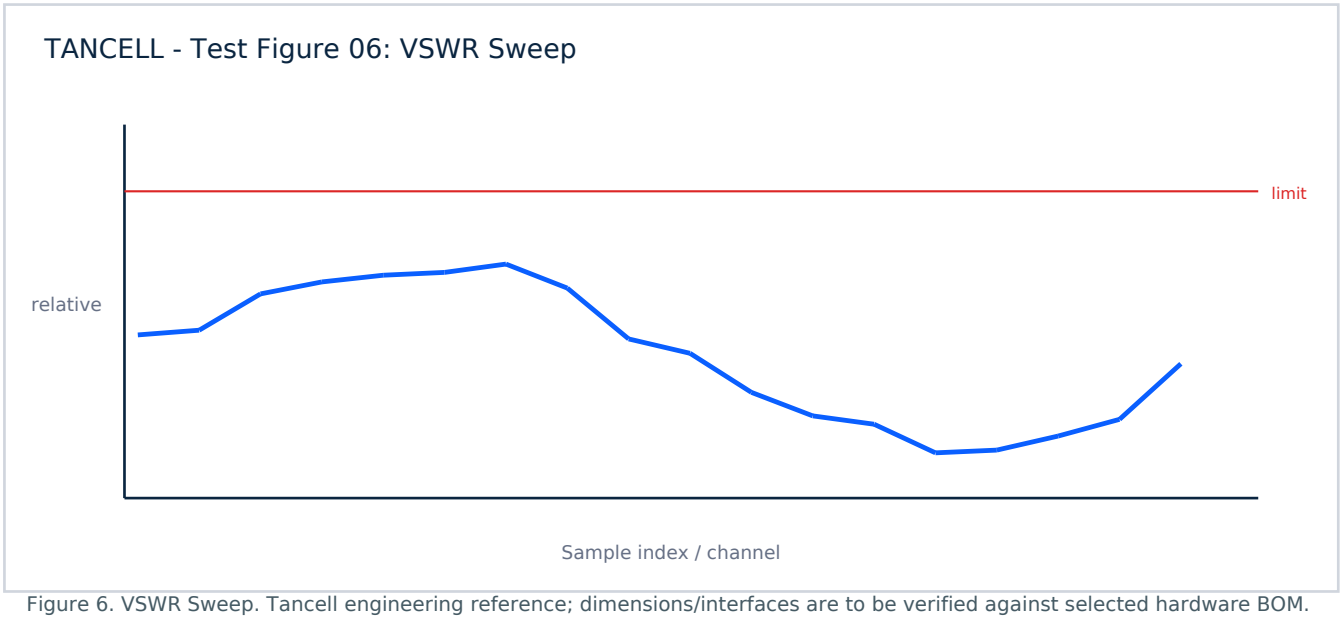

Figure 6. VSWR Sweep. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

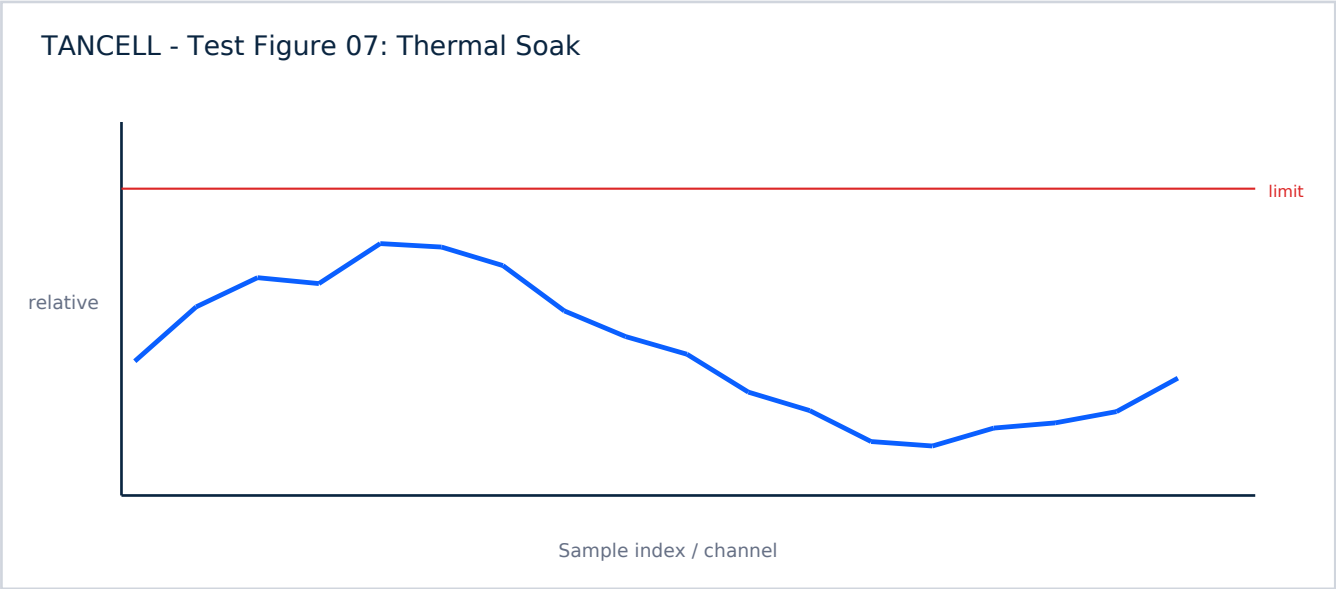

Figure 7. Thermal Soak. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

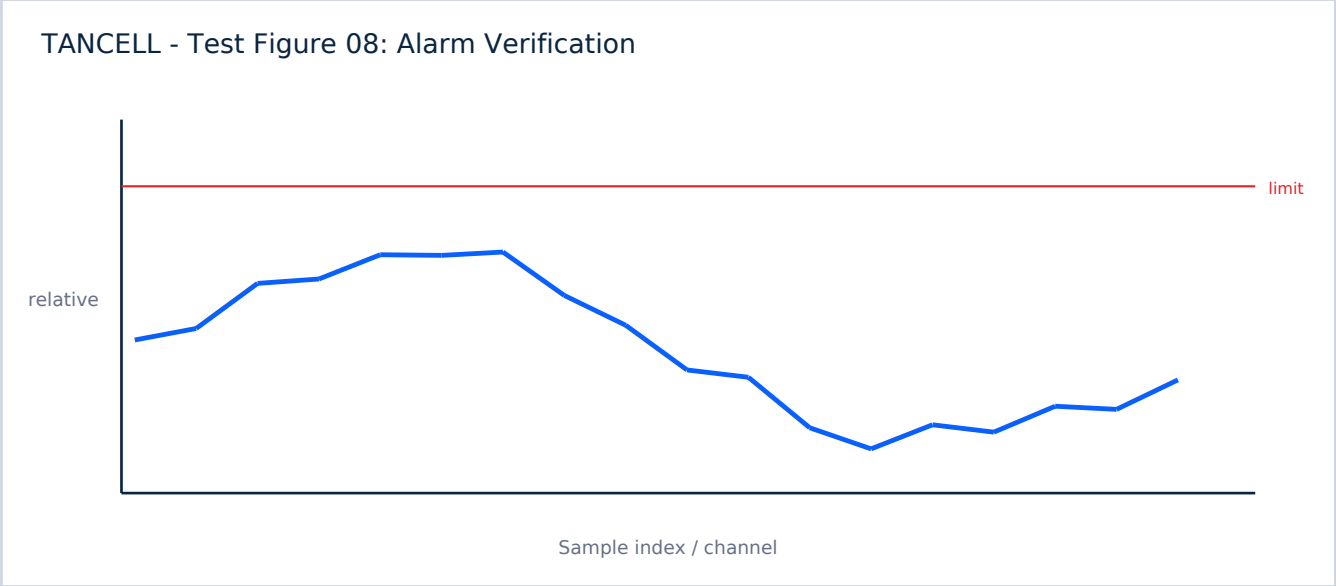

Figure 8. Alarm Verification. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

2. SAT - site acceptance

Sample commissioning plots for installed-site validation.

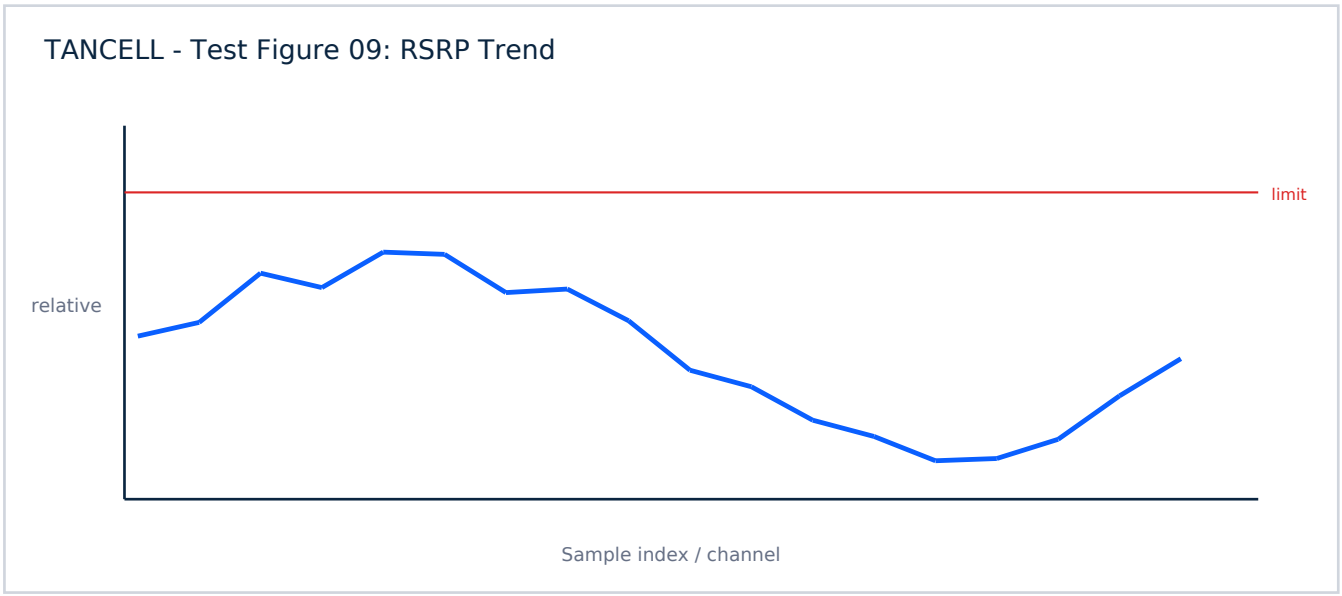

Figure 9. RSRP Trend. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

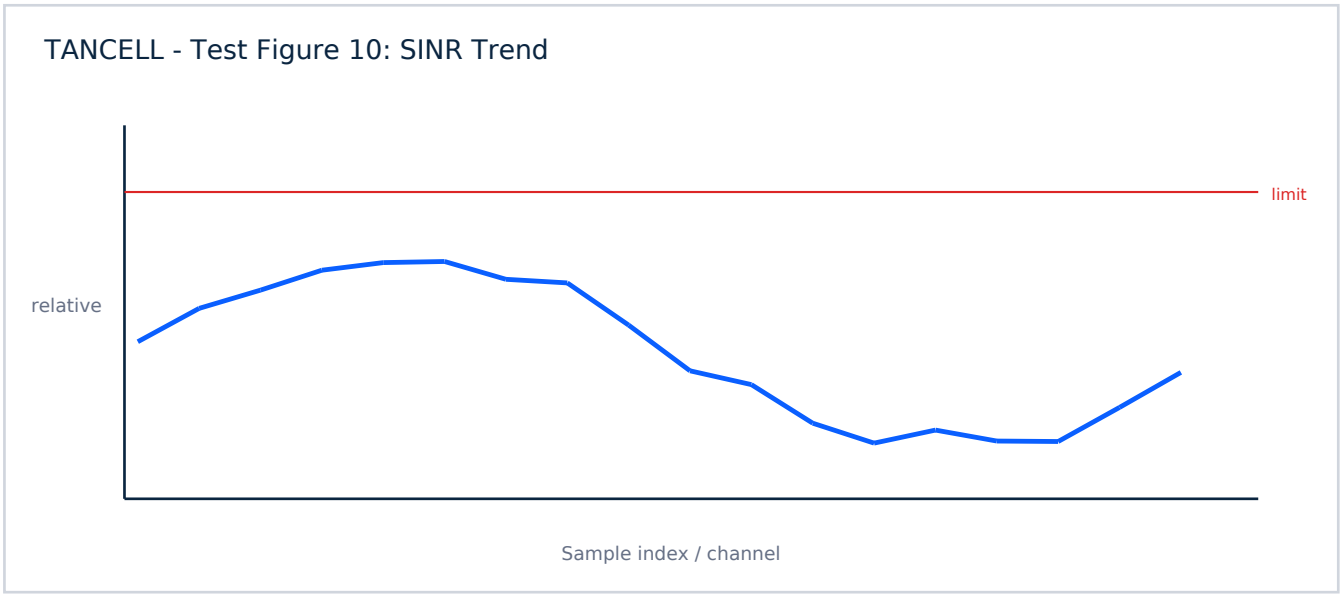

Figure 10. SINR Trend. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

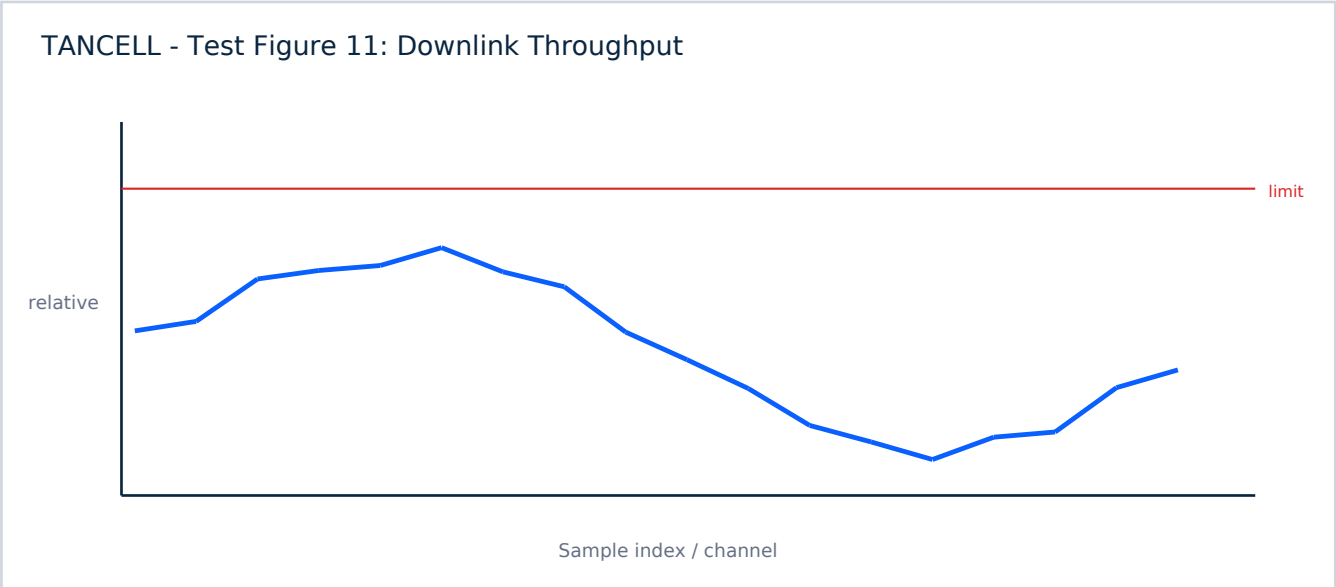

Figure 11. Downlink Throughput. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

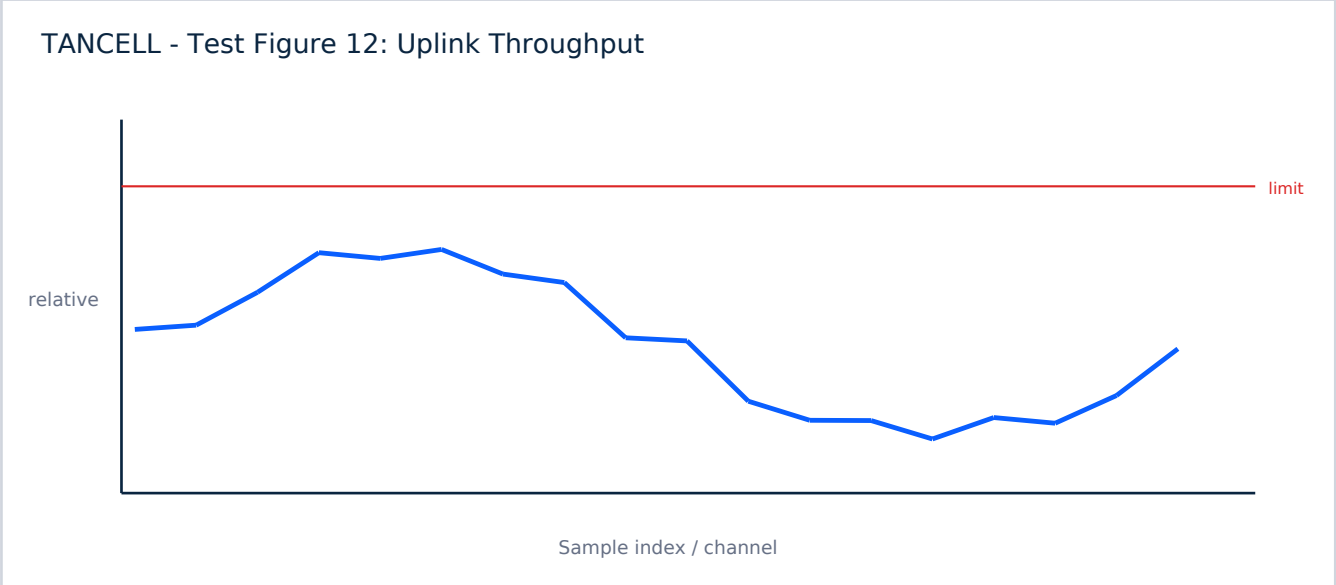

Figure 12. Uplink Throughput. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

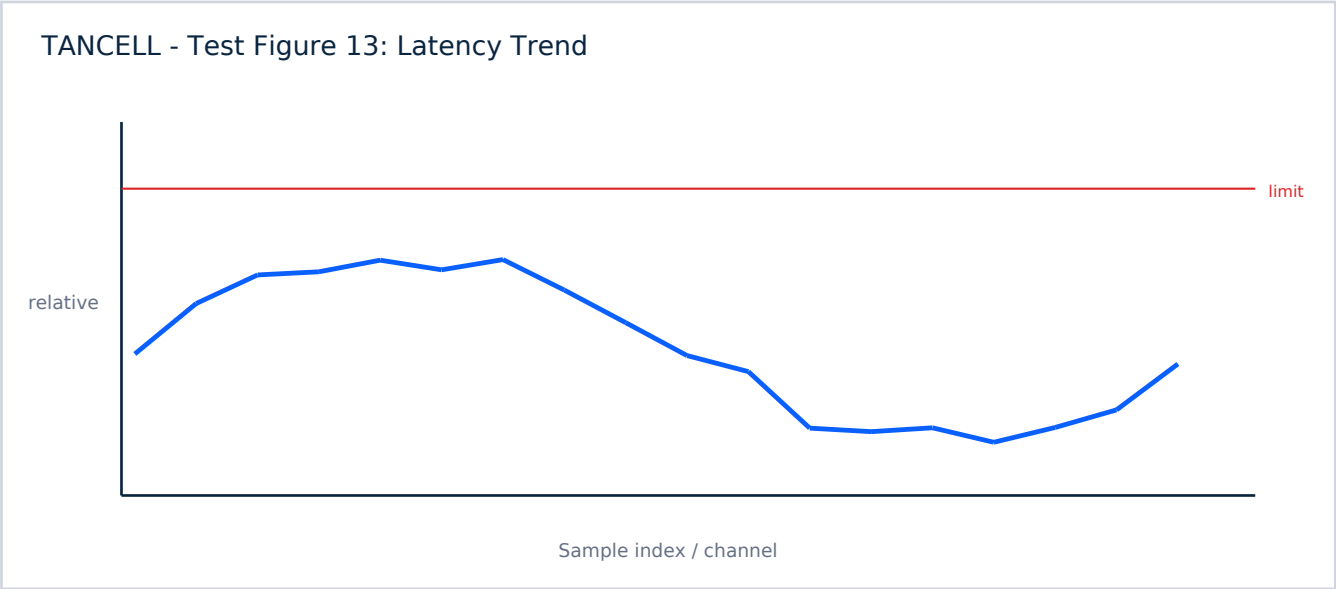

Figure 13. Latency Trend. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

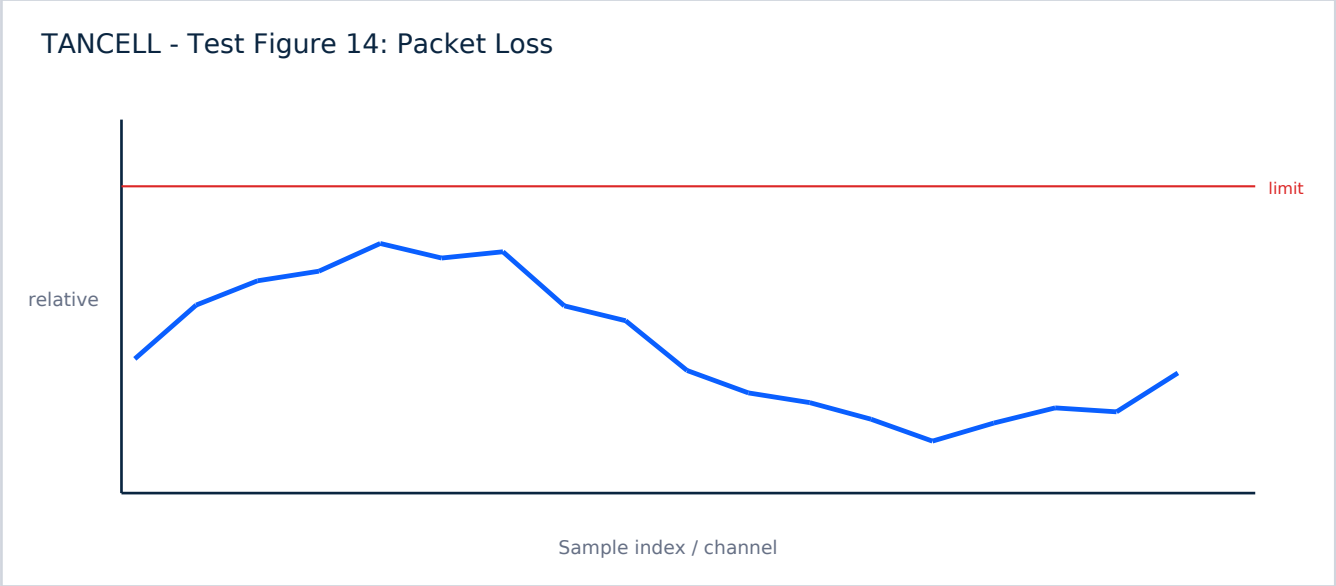

Figure 14. Packet Loss. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

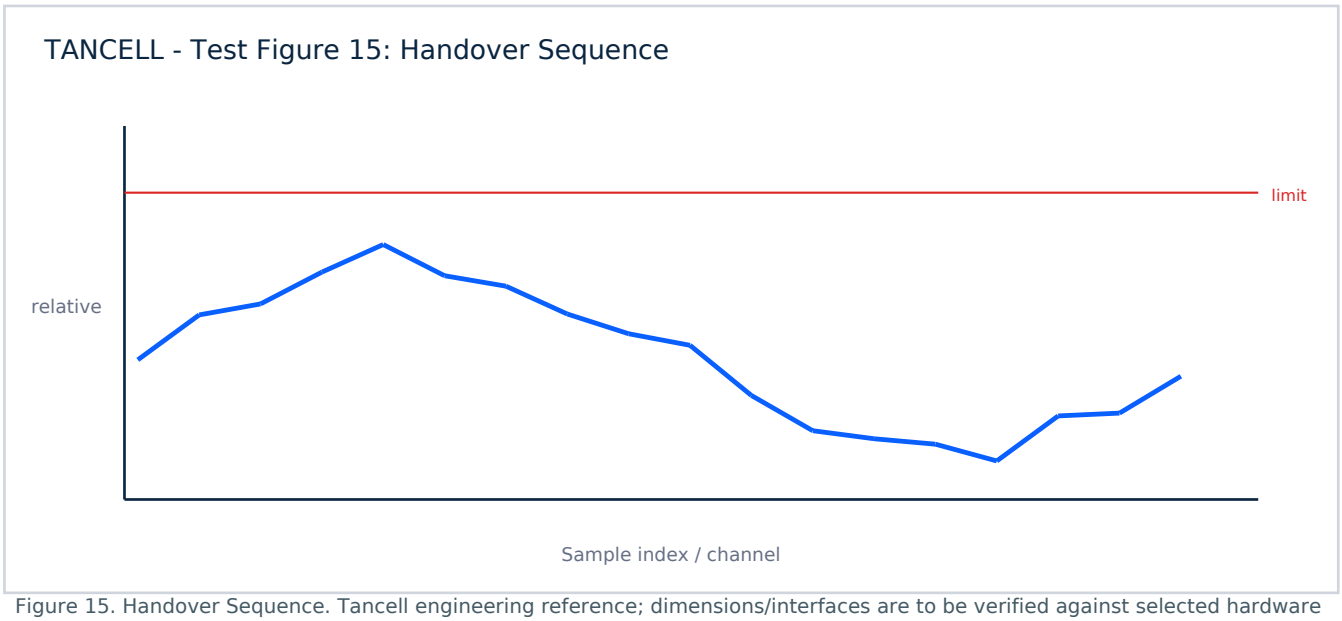

Figure 15. Handover Sequence. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

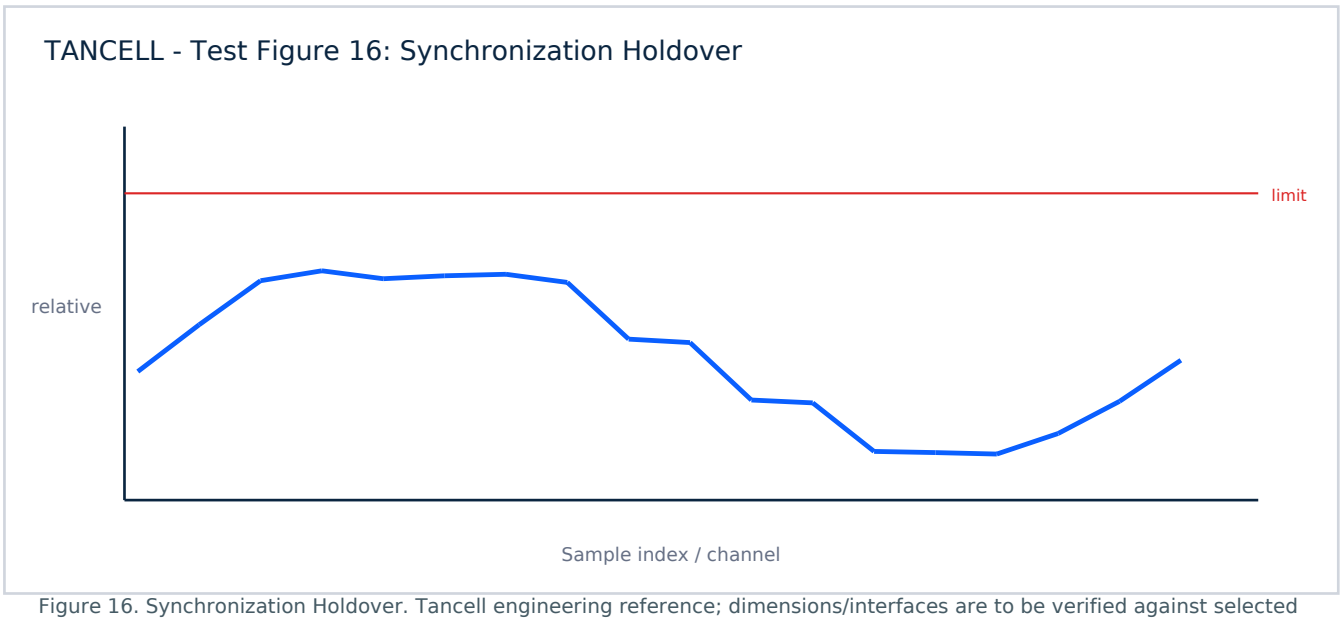

Figure 16. Synchronization Holdover. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

3. Reliability and environmental

Illustrative engineering verification records.

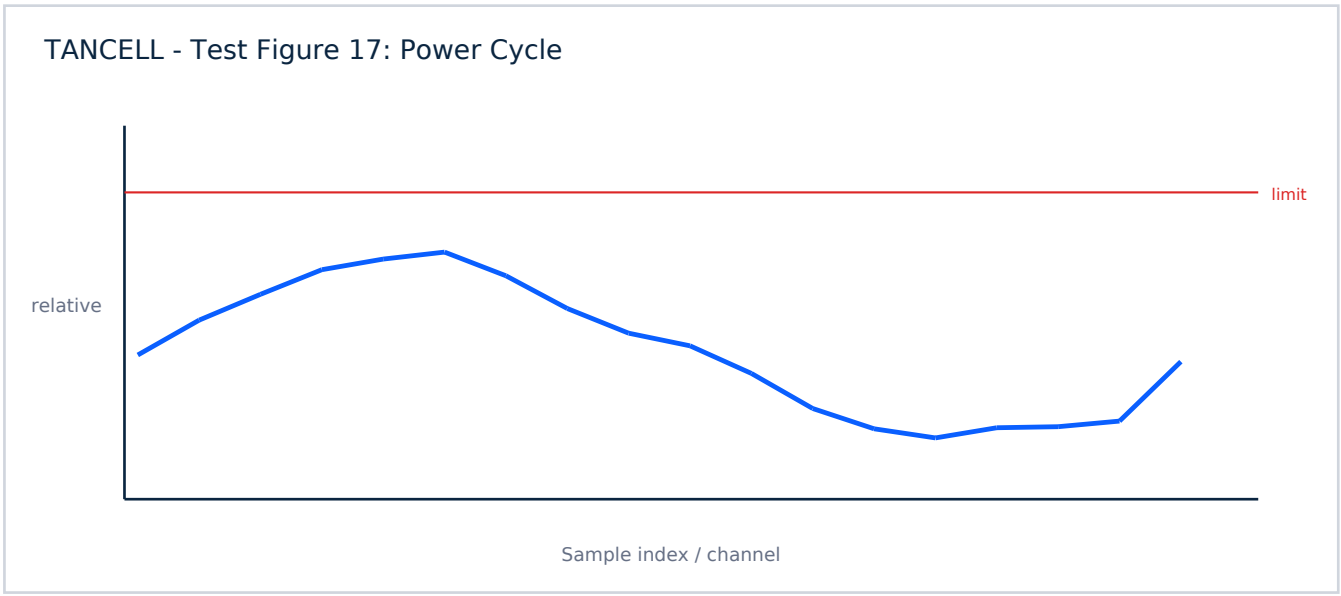

Figure 17. Power Cycle. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

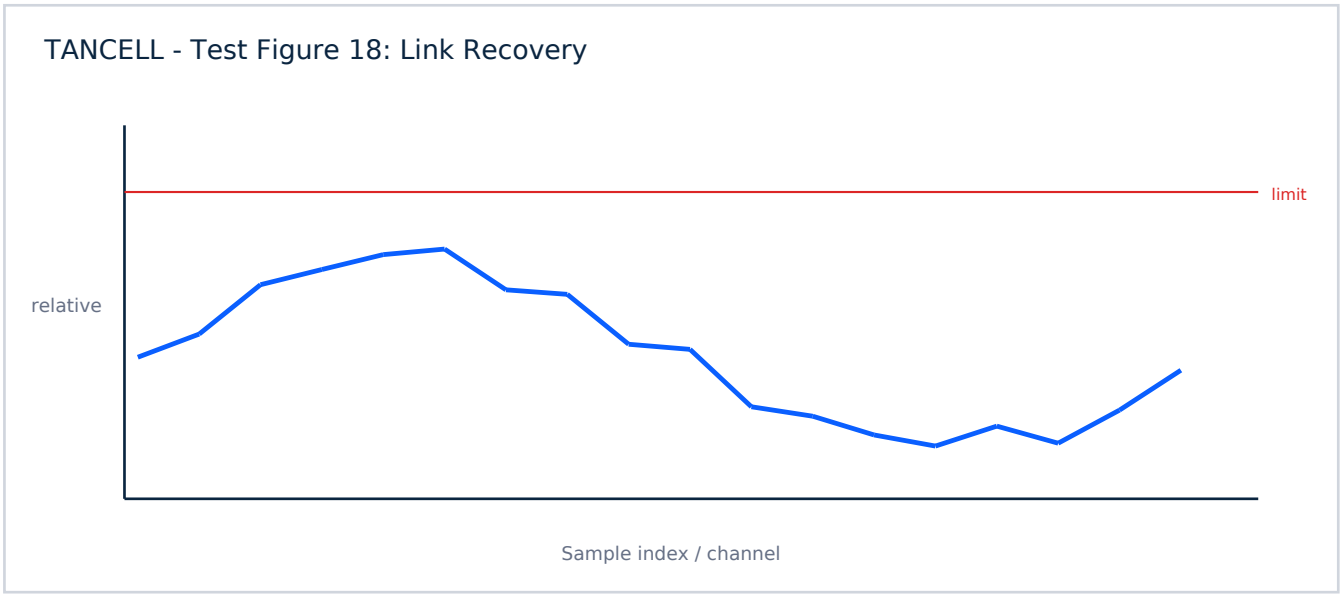

Figure 18. Link Recovery. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

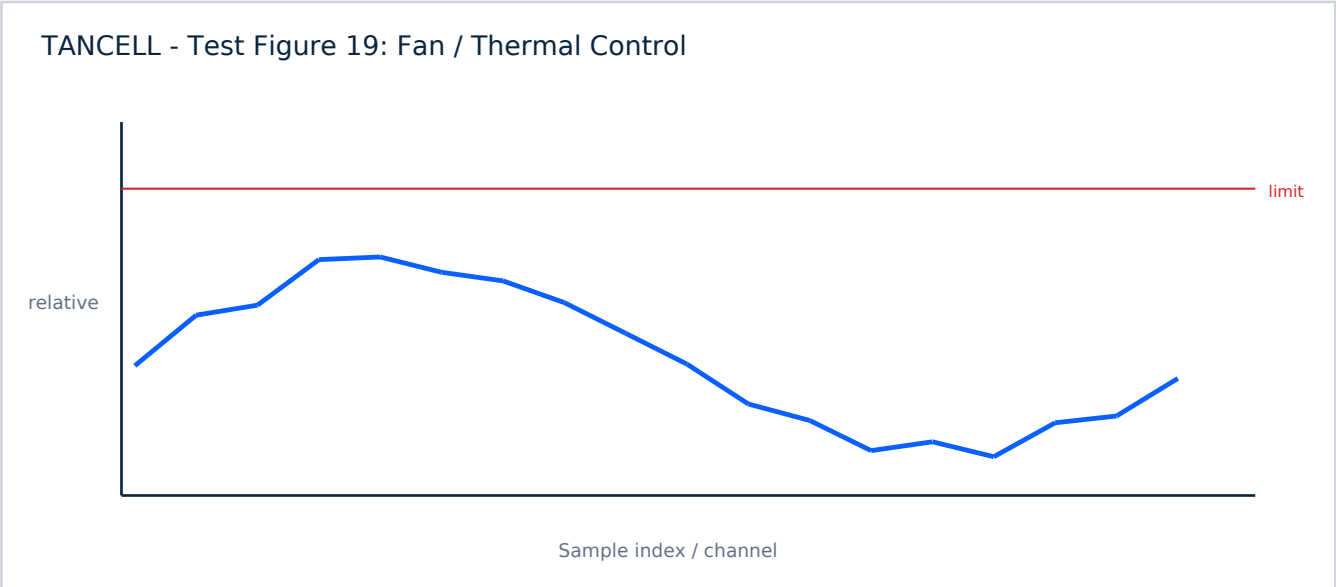

Figure 19. Fan / Thermal Control. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

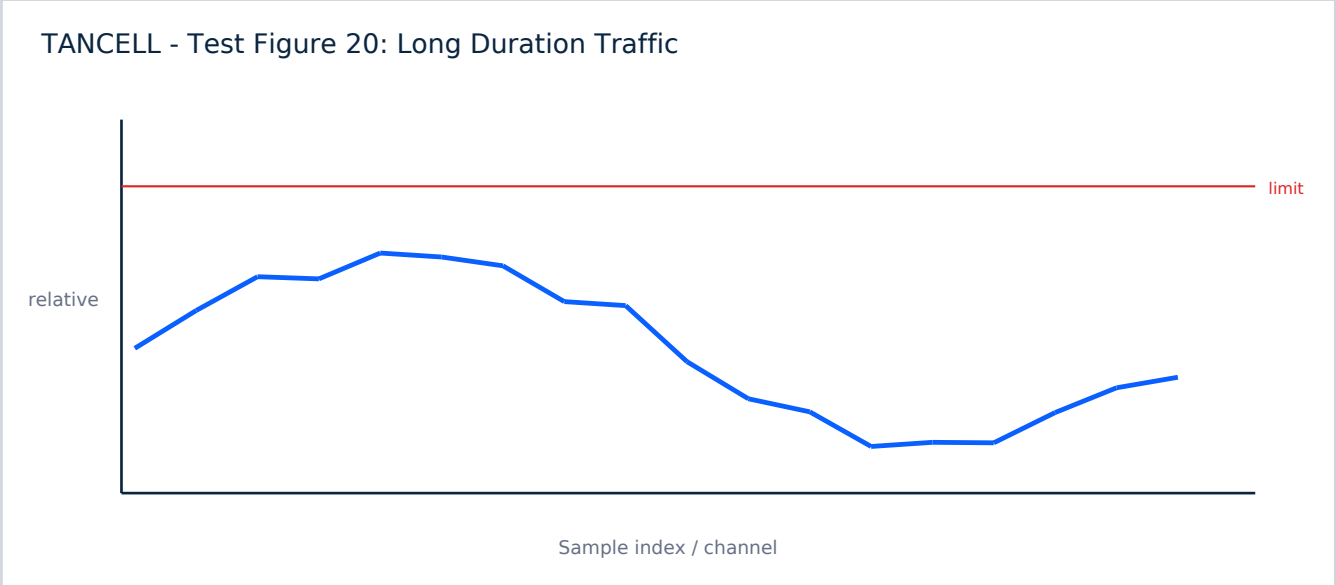

Figure 20. Long Duration Traffic. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

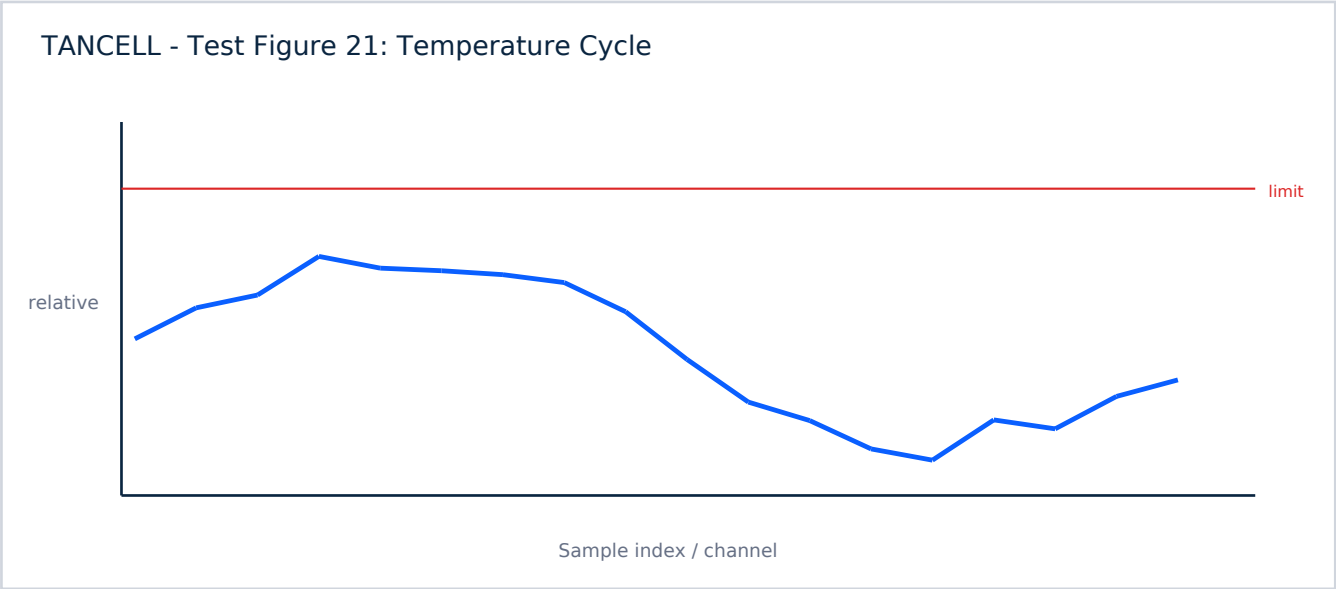

Figure 21. Temperature Cycle. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

Acceptance matrix

Test	Target / criterion	Sample result	Status
DC input	-40.5 to -57 VDC	-48.2 V	PASS
PTP lock	Locked, no critical alarm	Locked	PASS
Fronthaul	No CRC / link errors	0 errors / 30 min	PASS
VSWR	Per antenna/RF design	1.22:1 sample	PASS
Throughput	Project-specific KPI	1.84 Gbit/s DL sample	INFO
Latency	Project-specific KPI	8.7 ms sample	INFO
Thermal soak	No thermal shutdown	No shutdown sample	PASS
Alarm relay	All mapped alarms observed	Observed sample	PASS

All numerical results above are illustrative placeholders, not actual certified measurements.