

TANCELL

5G GSM Mobile Integration

Technical Design & Architecture

Document owner	Tancell Engineering
Revision	1.0
Date	14 September 2026
Classification	Technical / Engineering Reference
Standards basis	3GPP 5GS / 5G NR; O-RAN architecture concepts

Important: This package is a Tancell engineering reference design. Test values marked 'sample' or 'simulated' are not third-party certification results and must be replaced by measured laboratory/site data before regulatory submission or customer acceptance.

Document scope

This document set defines a vendor-neutral 5G mobile integration baseline covering UE-to-RAN connectivity, radio unit integration, transport/fronthaul, synchronization, DC power, grounding, mechanical installation, commissioning, alarms and acceptance testing. It is intended for engineering, tender, installation and FAT/SAT preparation.

Reference standards

Primary architecture reference: 3GPP TS 23.501 (5G System architecture). Radio/base-station reference: 3GPP TS 38.104 / ETSI TS 138 104. Open RAN transport drawings use O-RAN split 7-2x concepts. Always validate band, power, emissions, EMC, electrical safety and local spectrum/licensing requirements for the target country.

1. 5G system architecture

End-to-end logical integration from user equipment to radio access, transport, 5G core and edge services.

TANCELL - Drawing 01: 5G End-to-End Architecture

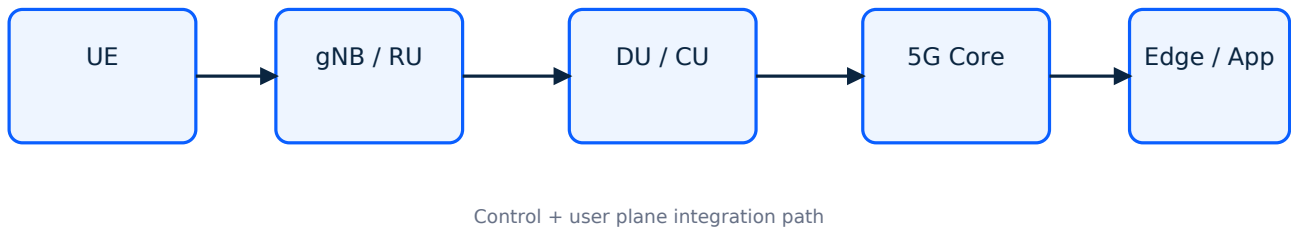


Figure 1. 5G End-to-End Architecture. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

TANCELL - Drawing 02: NSA/SA Integration

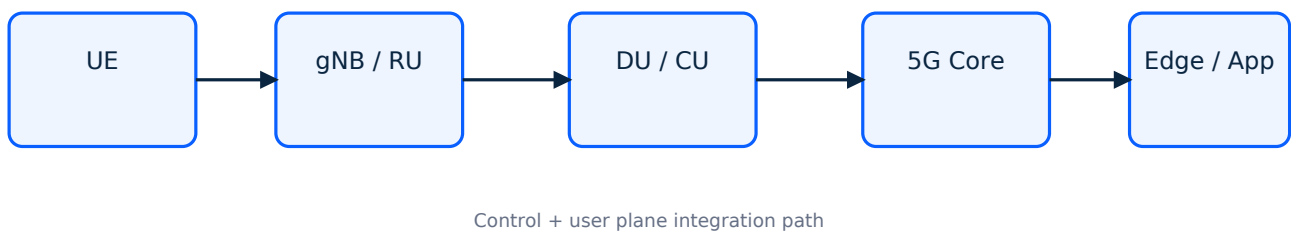


Figure 2. NSA/SA Integration. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

TANCELL - Drawing 03: User Plane Path



Control + user plane integration path

Figure 3. User Plane Path. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

TANCELL - Drawing 04: Control Plane Path



Control + user plane integration path

Figure 4. Control Plane Path. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

TANCELL - Drawing 05: Transport Network

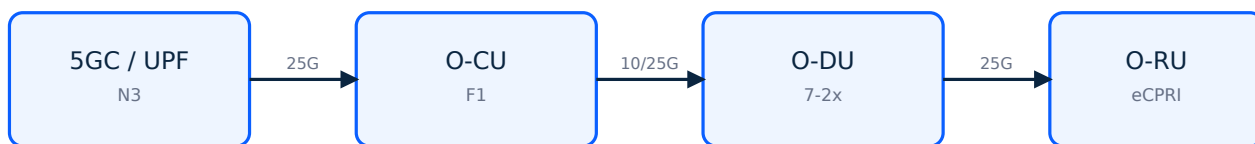


Figure 5. Transport Network. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

TANCELL - Drawing 06: Ethernet Fronthaul

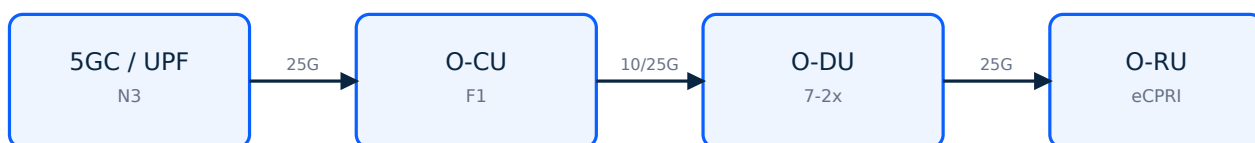


Figure 6. Ethernet Fronthaul. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

TANCELL - Drawing 07: Timing & Sync



Figure 7. Timing & Sync. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

TANCELL - Drawing 08: RF Antenna Chain

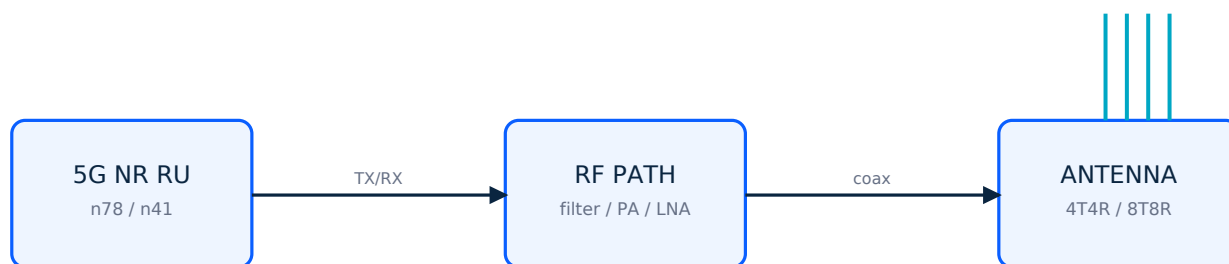


Figure 8. RF Antenna Chain. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

2. RAN and Open RAN integration

Reference decomposition for O-CU, O-DU and O-RU with fronthaul, synchronization and management paths.

TANCELL - Drawing 09: Fronthaul 7-2x

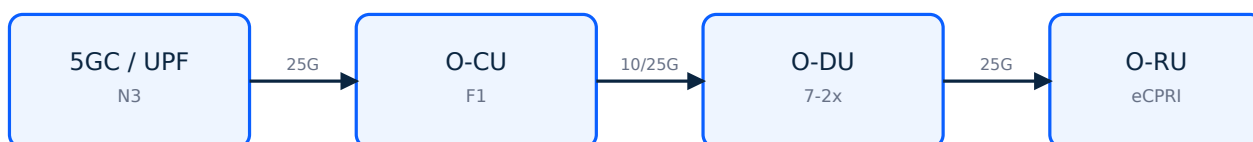


Figure 9. Fronthaul 7-2x. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

TANCELL - Drawing 10: Ethernet Transport

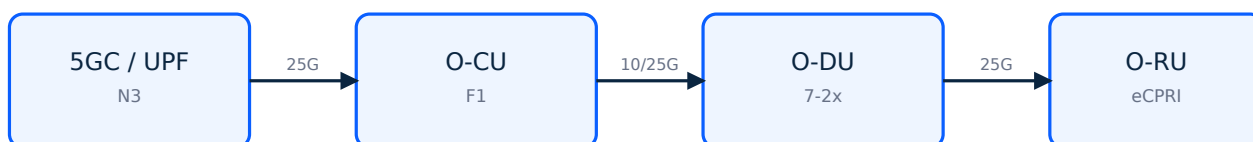


Figure 10. Ethernet Transport. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

TANCELL - Drawing 11: Timing Sync Distribution



Figure 11. Timing Sync Distribution. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

TANCELL - Drawing 12: RF Chain

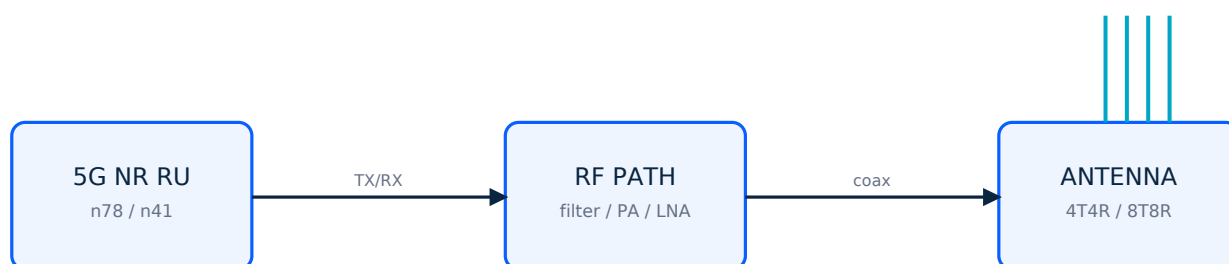


Figure 12. RF Chain. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

TANCELL - Drawing 13: Antenna Branching

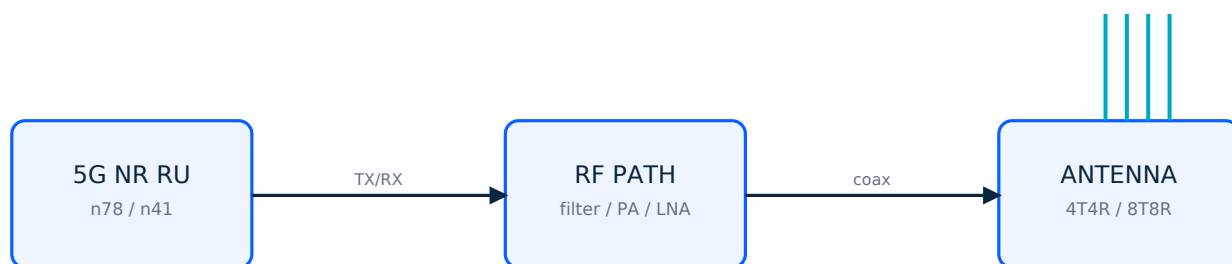


Figure 13. Antenna Branching. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

TANCELL - Drawing 14: Management Plane

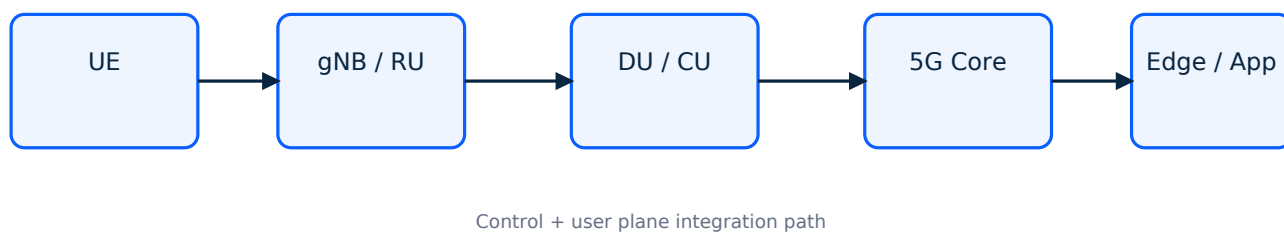


Figure 14. Management Plane. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

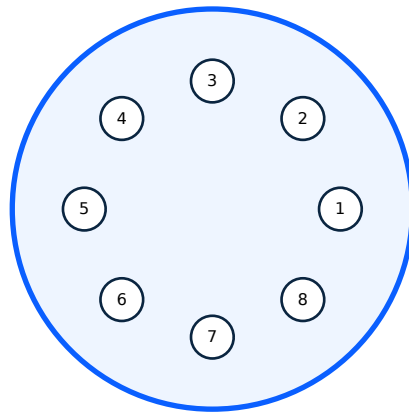
TANCELL - Drawing 15: Alarm Integration



Control + user plane integration path

Figure 15. Alarm Integration. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

TANCELL - Drawing 16: Connector Pinout



Example multi-pin service connector - engineering reference

Figure 16. Connector Pinout. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

3. Power, grounding and protection

48 VDC distribution, surge protection, grounding, cabinet feeds and redundancy concepts.

TANCELL - Drawing 17: Grounding Bonding

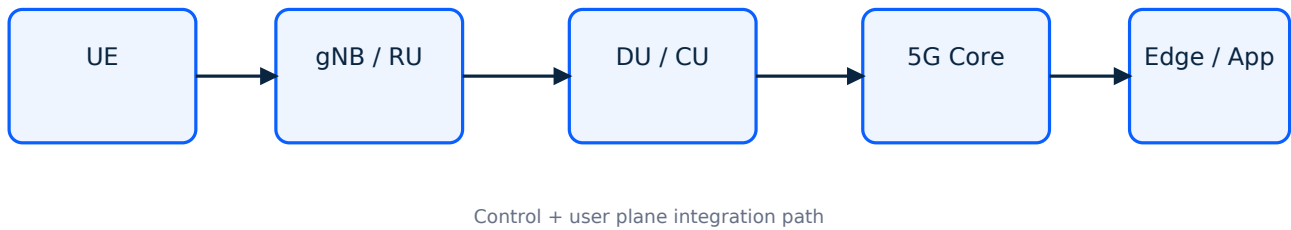


Figure 17. Grounding Bonding. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

TANCELL - Drawing 18: DC Breaker Layout

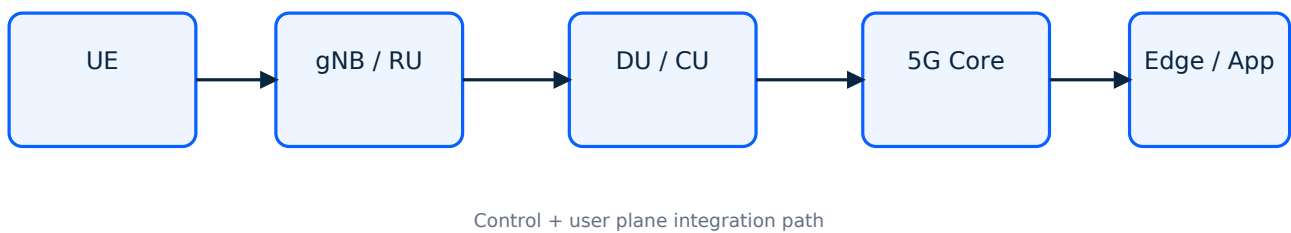


Figure 18. DC Breaker Layout. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

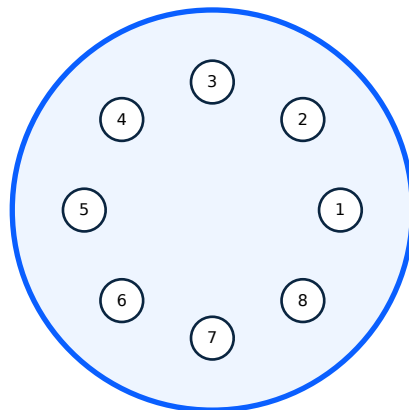
TANCELL - Drawing 19: Surge Protection



Control + user plane integration path

Figure 19. Surge Protection. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

TANCELL - Drawing 20: Connector Pinout



Example multi-pin service connector - engineering reference

Figure 20. Connector Pinout. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

TANCELL - Drawing 21: Power Monitoring

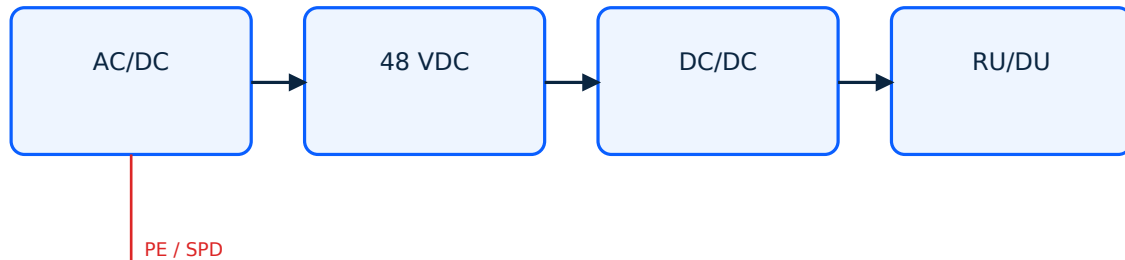


Figure 21. Power Monitoring. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

TANCELL - Drawing 22: Power Distribution

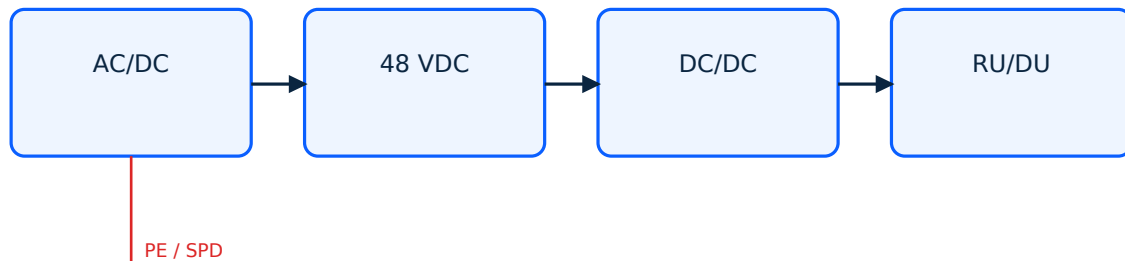


Figure 22. Power Distribution. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.

TANCELL - Drawing 23: Power A/B Redundancy

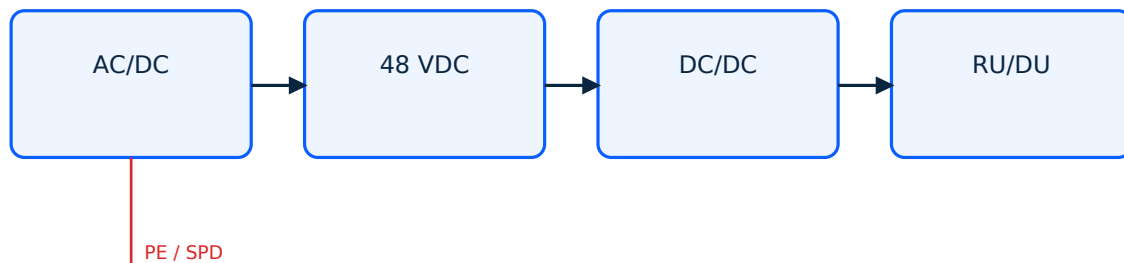


Figure 23. Power A/B Redundancy. Tancell engineering reference; dimensions/interfaces are to be verified against selected hardware BOM.